Experiment No: 1

P-N JUNCTION DIODE CHARACTERISTICS

AIM:

1. To plot Volt-Ampere Characteristics of Silicon P-N Junction Diode.
2. To find cut-in Voltage for Silicon P-N Junction diode.
3. To find static and dynamic resistances in both forward and reverse biased conditions for Si P-N Junction diode.

Components:

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diodes IN 4007(Si)</td>
<td>1</td>
</tr>
<tr>
<td>Resistor 1KΩ, 10KΩ</td>
<td>1</td>
</tr>
</tbody>
</table>

Equipment:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Regulated Power Supply</td>
<td>0-30V DC</td>
<td>1</td>
</tr>
<tr>
<td>Digital Ammeter</td>
<td>0-200μA/20mA</td>
<td>1</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>0-2V/20V DC</td>
<td>1</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory:

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a Junction called depletion region (this region is depleted off the charge carriers). This Region gives rise to a potential barrier $V_\gamma$ called Cut-in Voltage. This is the voltage across the diode at which it starts conducting. It can conduct beyond this Potential.

The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to anode (P-side) and –ve terminal of the input supply is connected to cathode (N-side) then diode is said to be forward biased. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current (injected minority current – due to holes crossing the junction and entering N-side of the diode, due to electrons crossing the junction and entering P-side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short-circuited switch.

If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased. In
this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on p-side and electrons on n-side tend to move away from the junction thereby increasing the depleted region. However the process cannot continue indefinitely, thus a small current called reverse saturation current continues to flow in the diode. This small current is due to thermally generated carriers. Assuming current flowing through the diode to be negligible, the diode can be approximated as an open circuited switch.

The volt-ampere characteristics of a diode explained by following equation:

\[ I = I_0 \left( e^{V/\eta T} - 1 \right) \]

where

- \( I \) = current flowing in the diode
- \( I_0 \) = reverse saturation current
- \( V \) = voltage applied to the diode
- \( V_T \) = volt-equivalent of temperature = kT/q = T/11,600 = 26mV (@ room temp).
- \( \eta = 1 \) (for Ge) and 2 (for Si)

It is observed that Ge diode has smaller cut-in-voltage when compared to Si diode. The reverse saturation current in Ge diode is larger in magnitude when compared to silicon diode.

**Circuit Diagram**

![Circuit Diagram](image-url)

**Fig (2) - Reverse Biased condition:**
Procedure:

Forward Biased Condition:

1. Connect the circuit as shown in figure (1) using silicon PN Junction diode.
2. Vary $V_f$ gradually in steps of 0.1 volts up to 5 volts and note down the corresponding readings of $I_f$.
3. Step Size is not fixed because of non-linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
4. Tabulate different forward currents obtained for different forward voltages.

Reverse biased condition:

1. Connect the circuit as shown in figure (2) using silicon PN Junction diode.
2. Vary $V_r$ gradually in steps of 0.5 volts up to 8 volts and note down the corresponding readings of $I_r$.
3. Tabulate different reverse currents obtained for different reverse voltages. ($I_r = \frac{V_R}{R}$, where $V_R$ is the Voltage across 10KΩ Resistor).

Observations

Si diode in forward biased conditions:

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>RPS Voltage</th>
<th>Forward Voltage across the diode $V_f$ (volts)</th>
<th>Forward current through the diode $I_f$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Si diode in reverse biased conditions:

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>RPS Voltage</th>
<th>Reverse Voltage across the diode $V_r$ (volts)</th>
<th>Reverse current through the diode $I_r$ (μA)</th>
</tr>
</thead>
</table>

Graph (Instructions):

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark:
   - + ve x-axis as $V_f$
   - - Ve x-axis as $V_r$
   - + Ve y-axis as $I_f$
   - - ve y-axis as $I_r$.

3. Mark the readings tabulated for Si forward biased condition in first Quadrant and Si reverse biased condition in third Quadrant.

Calculations from Graph:

- **Static forward Resistance** $R_{dc} = \frac{V_f}{I_f} \Omega$
- **Dynamic forward Resistance** $r_{ac} = \frac{\Delta V_f}{\Delta I_f}$ Ω
- **Static Reverse Resistance** $R_{dc} = \frac{V_r}{I_r}$ Ω
Dynamic Reverse Resistance \( r_{ac} = \frac{\Delta V_r}{\Delta I_r} \, \Omega \)

**Precautions:**
1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

**Result:**
1. Cut in voltage = ........ V 
2. Static forward resistance = ........ \( \Omega \) 
3. Dynamic forward resistance = ........ \( \Omega \) 

**VIVA-VOCE Questions**
1. How depletion region is formed in the PN junction?
2. What are trivalent and pentavalent impurities?
3. What is cut-in or knee voltage? Specify its value in case of Ge or Si?
4. What is maximum forward current and maximum reverse voltage? What is it required?
5. What is leakage current?
6. How does PN-junction diode acts as a switch?
7. What is the effect of temperature in the diode reverse characteristics?
8. What is break down voltage?
9. What is incremental resistance of a diode?
10. What is diode equation?
11. What is the value of \( V_T \) in the diode equation?
12. Explain the dynamic resistance of a diode?
13. Explain the phenomenon of breakdown in PN- diode?
14. What is an ideal diode? How does it differ from a real diode?
15. What are the specifications of a diode?
16. Temperature co-efficient of resistance of
   (i) Metals (ii) Intrinsic semiconductor (iii) Extrinsic semiconductor
   (iv) FET (v) BJT
17. What is the internal impedance of
   (i) Ideal current source (ii) Ideal voltage source (iii) Ammeter

**Specifications:**

**For Silicon Diode IN 4007:**

- Max. Forward Current = 1A
- Max. Reverse Current = 30\( \mu \)A
- Max. Forward Voltage = 0.8V
- Max. Reverse Voltage = 1000V
- Max. Power dissipation = 30mw
- Temperature = -65 to 200\(^\circ\)C
Ex
periment No: 2

ZENER DIODE CHARACTERISTICS

AIM:

1. To plot Volt-Ampere characteristics of Zener diode.
2. To find Zener break down voltage in reverse biased condition.
3. To calculate static and dynamic resistances of the Zener diode in both forward and reverse biased conditions (before, after break down voltages).

Components:

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zener Diode</td>
<td>1</td>
</tr>
<tr>
<td>Resistor 1KΩ</td>
<td>1</td>
</tr>
</tbody>
</table>

Equipment:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breadboard</td>
<td>-</td>
</tr>
<tr>
<td>Regulated DC power supply</td>
<td>0-30V</td>
</tr>
<tr>
<td>Ammeter</td>
<td>0-20mA</td>
</tr>
<tr>
<td>Voltmeter</td>
<td>0-20V</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
</tr>
</tbody>
</table>

Specifications:

Breakdown Voltage = 5.1V
Power dissipation = 0.75W
Max. Forward Current = 1A

Theory:

An ideal P-N Junction diode does not conduct in reverse biased condition. A **zener diode** conducts excellently even in reverse biased condition. These diodes operate at a precise value of voltage called break down voltage.

A zener diode when forward biased behaves like an ordinary P-N junction diode.

A zener diode when reverse biased can either undergo avalanche break down or zener break down.

**Avalanche break down:** If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction may
rupture covalent bonding between electrons. Such rupture leads to the generation of a large number of charge carriers resulting in **avalanche multiplication**.

**Zener breaks down:** If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces. Application of even a small voltage at the junction ruptures covalent bonding and generates large number of charge carriers. Such sudden increase in the number of charge carriers results in **zener mechanism**.

**Circuit Diagram:**

**Fig (1) – Forward Bias Condition:**

![Circuit Diagram for Forward Bias](image1)

**Fig (2) – Reverse Bias Condition:**

![Circuit Diagram for Reverse Bias](image2)

**Procedure:**

**Forward biased condition:**

1. Connect the circuit as shown in fig (1).
2. Vary $V_{zf}$ gradually steps of 0.1 volts up to 5volts and note down the corresponding readings of $I_{zf}$.
3. Tabulate different forward currents obtained for different forward voltages.

**Reverse biased condition:**
1. Connect the circuit as shown in fig (2).

2. Vary $V_{zr}$ gradually in steps of 0.5 volts up to 8 volts and note down the corresponding readings of $I_{zr}$.

3. Tabulate different reverse currents obtained for different reverse voltages.

**Observations:**

**Si diode in forward biased conditions:**

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>RPS Voltage</th>
<th>Forward Voltage across the diode $V_{zf}$ (volts)</th>
<th>Forward current through the diode $I_{zf}$ (mA)</th>
</tr>
</thead>
</table>

**diode in reverse biased conditions:**

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>RPS Voltage</th>
<th>Reverse Voltage across the diode $V_{zr}$ (volts)</th>
<th>Reverse current through the diode $I_{zr}$ (mA)</th>
</tr>
</thead>
</table>

**VOLTAGE REGULATION:**
LOAD REGULATION CHARACTERISTICS:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. By changing the load Resistance, kept constant I/P Voltage at 5V, 10 V, 15 V as per table given below. Take the readings of O/P Voltmeter (Vo=Vz).
3. Now by changing the I/P Voltage, kept constant load Resistance at 1K, 2K, 3K as per table given below. Take the readings of O/P Voltmeter (Vo=Vz).

<table>
<thead>
<tr>
<th>V1 (V)</th>
<th>R_L1=1KΩ VO (V)</th>
<th>R_L2=2KΩ VO (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
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<tr>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
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<tr>
<td>11</td>
<td></td>
<td></td>
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<tr>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S.No</th>
<th>R_L (Ω)</th>
<th>V1= 5V VO (V)</th>
<th>V1= 10V VO (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>900</td>
<td></td>
<td></td>
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<tr>
<td>6</td>
<td>1K</td>
<td></td>
<td></td>
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<tr>
<td>7</td>
<td>3K</td>
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<td></td>
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<tr>
<td>8</td>
<td>5K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>7K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>10K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Instructions:**
1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.

2. Now mark:
   - +ve x-axis as $V_{Zf}$
   - -ve x-axis as $V_{Zr}$
   - +ve y-axis as $I_{Zf}$
   - -ve y-axis as $I_{Zr}$

3. Mark the readings tabulated for zener diode forward biased condition in first Quadrant and Zener diodes reverse biased condition in third Quadrant.

**Calculations from Graph:**

![Graph diagram]

- Static forward Resistance $R_{dc} = \frac{V_{zf}}{I_{zf}}$
- Dynamic forward Resistance $r_{ac} = \frac{\Delta V_{zf}}{\Delta I_{zf}}$
- Static Reverse Resistance $R_{dc} = \frac{V_{zr}}{I_{zr}}$
- Dynamic Reverse Resistance $r_{ac} = \frac{\Delta V_{zr}}{\Delta I_{zr}}$

**Precautions:**

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

**Inference:**

1. In the forward biased mode the zener diode operates as a p-n diode.
2. In the reverse biased mode zener diode has large breakdown voltage and though the current increases the voltage remains constant. Thus it acts as a voltage regulator.

**Result:**

a. The zener diode characteristics have been studied.
b. The zener resistance at the breakdown voltage was found to be = ………
1. What is a zener diode? How it differs from an ordinary diode?
2. Explain the concept of zener breakdown?
3. What is avalanche breakdown?
4. What type of biasing must be used when a zener diode is used as a regulator?
5. Current in a 1W – 10V zener diode must be limited to a maximum of what value?
6. What are the advantages of zener diode?
7. State reason why an ordinary diode suffers avalanche breakdown rather than zener breakdown?
8. If impurities in a zener diode increases what happens to the forward voltage?
9. Can zener be used as a rectifier?
10. Specifications of the zener diode?
Experiment No: 3

COMMON BASE CONFIGURATION

AIM: To study the input and output characteristics of a transistor in common base configuration.

Components:

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor CL 100S</td>
<td>1</td>
</tr>
<tr>
<td>Resistor 1KΩ</td>
<td>2</td>
</tr>
</tbody>
</table>

Equipment:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Regulated Power Supply</td>
<td>0-30V DC</td>
<td>2</td>
</tr>
<tr>
<td>Digital Ammeter</td>
<td>0-20mA</td>
<td>2</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>0-20V DC</td>
<td>2</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Specifications:
For Transistor CL 100S: -
Max. Collector Current = 0.1A
V_{CEO \text{ max}} = 50V

Pin Assignment of Transistor:

![Emitter Base Collector Diagram]
Circuit Diagram:

1) INPUT CHARACTERISTICS:

![Circuit Diagram for Input Characteristics](image1)

2) OUTPUT CHARACTERISTICS:

![Circuit Diagram for Output Characteristics](image2)

Theory:

Bipolar junction transistor (BJT) is a 3 terminal (emitter, base, and collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely emitter junction and collector junction.

The basic circuit diagram for studying input characteristics is shown in fig (1). The input is applied between emitter and base and the output is taken from collector and base. Here base of the transistor is common to both input and output and hence the name common base configuration. Input characteristics are obtained between the input current and input voltage at constant output voltage. It is plotted between $V_{EB}$ and $I_E$ at constant $V_{CB}$ in CB configuration.
Output characteristics are obtained between the output voltage and output current keeping input current constant. It is plotted between $V_{CB}$ and $I_C$ at Constant $I_E$ in CB configuration.

**Procedure:**

**Input Characteristics**

1. Make connections as per circuit diagram fig (1).
2. Keep output voltage $V_{CB} = 0 \text{V}$ by varying $V_{EE}$.
3. Varying $V_{EE}$ gradually, note down both emitter current $I_E$ and emitter-base voltage ($V_{EB}$).
4. Repeat above procedure (step 3) for $V_{CB} = 5 \text{V}$.

**Output Characteristics**

1. Make connections as per circuit diagram fig (2).
2. By varying $V_{EE}$ keep the emitter current $I_E = 5 \text{mA}$.
3. Varying $V_{CC}$ gradually, note down the readings of collector-current ($I_C$) and collector-base voltage ($V_{CB}$).
4. Repeat above procedure (step 3) for $I_E = 10 \text{mA}$.

**Observations:**

<table>
<thead>
<tr>
<th>$V_{CB} = 0 \text{V}$</th>
<th>$V_{CB} = 5 \text{V}$</th>
<th>$I_E = 5 \text{mA}$</th>
<th>$I_E = 10 \text{mA}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_E$ (mA)</td>
<td>$V_{EB}$ (V)</td>
<td>$I_E$ (mA)</td>
<td>$V_{EB}$ (V)</td>
</tr>
</tbody>
</table>
1. Plot the input characteristics for different values of $V_{CB}$ by taking $V_{EB}$ on y-axis and $I_E$ on x-axis.
2. Plot the output characteristics by taking $V_{CB}$ on x-axis and $I_C$ on y-axis taking $I_E$ as a parameter.
Calculations from graph:

1. **Input resistance**: To obtain input resistance find $\Delta V_{EB}$ and $\Delta I_E$ for a constant $V_{CB}$ on one of the input characteristics.
   
   \[ R_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad (V_{CB} = \text{constant}) \]

2. **Output resistance**: To obtain output resistance find $\Delta I_c$ and $\Delta V_{CB}$ at constant $I_E$.
   
   \[ R_o = \frac{\Delta V_{CB}}{\Delta I_c} \quad (I_E = \text{constant}) \]

Inference:

1. Input resistance is in the order of tens of ohms since emitter-base junction is forward biased.
2. Output resistance is in the order of hundreds of kilo-ohms since collector-base junction is reverse biased.
3. Higher is the value of $V_{CB}$, smaller is the cut in voltage.
4. Increase in the value of $I_B$ causes saturation of transistor at small voltages.

Precautions:

1. While doing the experiment do not exceed the ratings of the Transistor. This may lead to damage the transistor.
2. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
3. Do not switch ON the power supply unless you have checked the Circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of The transistor.

Result:

1. Input Resistance ($R_i$) = ............Ω
2. Output Resistance ($R_o$) = ............Ω
3. $\alpha=I_c/I_e \quad |V_{CE}=\text{constant} \quad ______$

**VIVA-VOCE Questions**

1. How to test the diode & transistor-using multimeter?
2. What are the uses of a common base configuration?
3. What is a buffer?
4. Why CB configuration is called constant current source?
5. What is the maximum value of ‘$\alpha$’?
6. Draw the symbol of NPN and PnP transistors?
7. What is base-width modulation?
8. Why is base made thin?
9. What is the significance of arrow in the transistor symbol?
10. Define current amplification factor?
11. Compare input and output impedance of CB configuration with that of CC configuration?
12. What is the function of a transistor?
13. Define $\beta$? What is the range of $\beta$?
14. Why CC configuration is called as emitter follower?
Experiment No: 4

COMMON EMITTER CONFIGURATION

**AIM:** To study the input and output characteristics of a transistor in common emitter configuration.

**Components:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor CL 100S</td>
<td>1</td>
</tr>
<tr>
<td>Resistor 220Ω</td>
<td>1</td>
</tr>
<tr>
<td>Resistor 560Ω</td>
<td>1</td>
</tr>
</tbody>
</table>

**Equipment:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Regulated Power Supply</td>
<td>0-30V DC</td>
<td>2</td>
</tr>
<tr>
<td>Digital Ammeter</td>
<td>0-20mA /0-200µA</td>
<td>1</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>0-2V/20V DC</td>
<td>1</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Specifications:**

For Transistor **CL 100S:**

- Max. Collector Current = 0.1A
- $V_{CEO}$ max = 50V

**Pin assignment of Transistor:**

![Pin assignment diagram]
Circuit Diagram:

1) INPUT CHARACTERISTICS

![Input Circuit Diagram]

2) OUTPUT CHARACTERISTICS:

![Output Circuit Diagram]

Theory:
The basic circuit diagram for studying input and output characteristics are shown in fig (1) & fig (2). In this the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between $V_{BE}$ and $I_B$ at constant $V_{CE}$ in CE configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between $V_{CE}$ and $I_C$ at constant $I_B$ in CE configuration.

Procedure:

Input Characteristics

4. Make the connections as per circuit diagram fig (1).
5. Keep output voltage $V_{CE} = 0V$ by varying $V_{CC}$.

6. Varying $V_{BB}$ gradually, note down both base current $I_B$ and base - emitter voltage ($V_{BE}$).

4. Repeat above procedure (step 3) for $V_{CE} = 5V$.

**Output Characteristics**

5. Make the connections as per circuit diagram fig (2).

6. By varying $V_{BB}$ keep the base current $I_B = 20 \mu A$.

7. Varying $V_{CC}$ gradually, note down the readings of collector-current ($I_C$) and collector-emitter voltage ($V_{CE}$).

8. Repeat above procedure (step 3) for $I_E = 40 \mu A$.

**Observations:**

<table>
<thead>
<tr>
<th>$I_B$ ($\mu A$)</th>
<th>$V_{BE}$ (V)</th>
<th>$I_B$ ($\mu A$)</th>
<th>$V_{BE}$ (V)</th>
<th>$I_B$ = 20$\mu A$</th>
<th>$I_C$ (mA)</th>
<th>$V_{CE}$ (V)</th>
<th>$I_C$ (mA)</th>
<th>$I_B$ = 40$\mu A$</th>
<th>$I_C$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE} = 0V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CE} = 5V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Input Characteristics**

**Output Characteristics**
**Expected graph:**

3. Plot the input characteristics by taking $V_{BE}$ on Y-axis and $I_B$ on X-axis at constant $V_{CE}$.
4. Plot the output characteristics by taking $V_{CE}$ on Y-axis and $I_C$ on X-axis by taking $I_B$ as a parameter.

**Calculations from graph:**

2. **Input resistance:** To obtain input resistance find $\Delta V_{BE}$ and $\Delta I_B$ at constant $V_{CE}$ on one of the input characteristics.
   Then $R_i = \frac{\Delta V_{BE}}{\Delta I_B}$ ($V_{CE}$ constant)

2. **Output resistance:** To obtain output resistance, find $\Delta I_C$ and $\Delta V_{CE}$ at Constant $I_B$.
   $R_o = \frac{\Delta V_{CE}}{\Delta I_C}$ ($I_B$ constant)

**Inference:**

1. Medium Input and Output resistances.
2. Smaller value of $V_{CE}$ comes earlier cut-in-voltage.
3. Increase in the value of $I_B$ causes saturation of the transistor at an Earlier voltage.

**Precautions:**

4. While doing the experiment do not exceed the ratings of the Transistor. This may lead to damage the transistor.
5. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
6. Do not switch ON the power supply unless you have checked the Circuit connections as per the circuit diagram.
7. Make sure while selecting the emitter, base and collector terminals of the transistor.

**Result:**

1. Input Resistance ($R_i$) = ……………Ω
2. Output Resistance ($R_o$) = ........... $\Omega$

3. $\beta = \frac{I_c}{I_B}$ | $v_{ce}$ = constant

**Viva-Voce Questions**

1. Two discrete diodes connected back-to-back cannot work as a transistor, why?

2. For amplification, CE configuration is preferred, why?

3. To operate a transistor as amplifier, the emitter junction is forward biased and the collector junction is reversed biased, why?

4. With the rise in temperature, the leakage collector current increases, why?

5. An electronic device transistor is named as transistor, why?

6. Most of the transistor are **NPN** type and not **PnP**, why?

7. The forward resistance of emitter junction is slightly less than forward resistance of collector junction, why?
Experiment No: 5

HALF WAVE RECTIFIER WITH & WITHOUT FILTERS

AIM: Study of Half – wave rectifier with & without Filter and to finds Ripple Factor.

EQUIPMENT:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer</td>
<td>9-0-9V/12-0-12V</td>
<td>1</td>
</tr>
<tr>
<td>Bread Board</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Digital Multimeter</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Resistor</td>
<td>1kΩ,10kΩ</td>
<td>1</td>
</tr>
<tr>
<td>Connecting wires</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

THEORY:

The conversion of AC into DC is called Rectification. Electronic devices can convert AC power into DC power with high efficiency
Consider the given circuit. Assume the diode to be ideal i.e. $V_f = 0$, $R_t = \infty$, $R_s = 0$. During the positive half cycle, the diode is forward biased and it conducts and hence a current flows through the load resistor. During the negative half cycle, the diode is reverse biased and it is equivalent to an open circuit, hence the current through the load resistance is zero. Thus the diode conducts only for one half cycle and results in a half wave rectified output.

MATHEMATICAL ANALYSIS

(Neglecting $R_f$ and $R_s$)
Let $V_{ac} = V_m \sin \omega t$ is the input AC signal, the current $I_{ac}$ flows only for one half cycle i.e. from $\omega t = 0$ to $\omega t = \pi$, where as it is zero for the duration $\pi \leq \omega t \leq 2\pi$
Therefore, $I_{ac} = \frac{V_{ac}}{R} = \frac{V_m \sin \omega t}{R}$

$= I_m \sin \omega t \quad 0 \leq \omega t \leq \pi$

$= 0 \quad \pi \leq \omega t \leq 2\pi$

Where $I_m = \text{maximum value of current}$
$V_m = \text{maximum value of voltage}$

AVERAGE OR DC VALUE OF CURRENT

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_m (\sin \omega t) \, dt$$
\[
I_{dc} = \frac{1}{2\pi} \left[ \frac{\pi}{\sin \omega t} \int_0^{2\pi} \frac{2\pi}{\dot{I}} \dot{I} \, d\omega t \right] = \frac{\text{Im}}{\pi}
\]

Similarly

\[
V_{dc} = \frac{V_m}{\pi}
\]

**The RMS VALUE OF CURRENT**

\[
I_{\text{rms}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_{ac}^2 \, d\omega t}
\]

\[
= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_{m}^2 \sin^2 \omega t \, d\omega t}
\]

\[
= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \frac{1}{2} \cdot 1 - \cos 2\omega t \, d\omega t} = \frac{I_m}{2}
\]

Similarly

**RIPPLE FACTOR:**

\[
V_{\text{rms}} = \frac{V_m}{2}
\]

The output of a half-wave rectifier consists of some undesirable ac components known as ripple. These can be removed using suitable filter circuits.

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol

\[
\gamma = \frac{V_{ac}}{V_{dc}}
\]

\[
V_{\text{rms}}^2 = V_{ac}^2 + V_{dc}^2
\]

\[
\gamma = \sqrt{\frac{V_{\text{rms}}^2 - V_{dc}^2}{V_{dc}}}
\]

Converting \( V_{\text{rms}} \) and \( V_{dc} \) into its corresponding \( V_m \) value, we get

\[
\gamma = 1.21
\]

**RECTIFICATION FACTOR:**

The ratio of output DC power to the input AC power is defined as efficiency

Output power = \( I_{dc}^2 R \)

Input power = \( I_{\text{rms}}^2 (R + R_f) \)
Where $R_f$ – forward resistance of the diode

\[
\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R}{I_{rms}^2 (R+R_f)}
\]

\[
\eta = \frac{4}{\pi^2} \times \frac{R}{R + R_f}
\]

= 40.5% (if $R_f \ll R$, $R_f$ can be neglected).

**CIRCUIT DIAGRAM:**

Half Wave Rectifier (with out filter):

---

**CIRCUIT DIAGRAM:**

Half Wave Rectifier (with out filter):
**PROCEDURE:**

1. Make connections as per the Circuit Diagram.
2. Note down the AC and DC Voltages and Currents without Filter and with Load.
3. And again observe the AC and DC Voltages and Currents with L & Π Filters and with load.
4. Observe the Voltage across the secondary of the Transformer.

**Tabular Column:**

\[ V_{ac} = \text{______ (Voltage across the secondary of the transformer)} \]

<table>
<thead>
<tr>
<th>Condition</th>
<th>( V_{ac} )</th>
<th>( V_{dc} )</th>
<th>( V_m )</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without Filter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>With C Filter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CALCULATIONS:

Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$

EXPECTED WAVEFORMS:

Input Waveform

HWR WITHOUT FILTER:

HWR WITH FILTER:

$V_R = $ Ripple Voltage
RESULT: -

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without filter</th>
<th>With c - Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple Factor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VIVA-VOCE Questions

1. Why are rectifiers used with a filter at their output?
2. What is the voltage regulation of the rectifier?
3. What is the ideal value of regulation?
4. What does no load condition refer to?
5. What are the advantages of bridge rectifier?
6. What are the advantages and disadvantages of capacitor filter?
7. What are the applications of rectifiers?
8. What is the regulation for a
   (i) Half - wave circuit (ii) Full-wave circuit
9. What is PIV? State it value in case of (i) Half wave (ii) Full wave (iii) Bridge rectifier.
10. What is the output signal frequency in case of (i) Half wave (ii) Full wave (iii) Bridge rectifier?
Experiment No: 6

FULLWAVE RECTIFIER WITH & WITHOUT FILTERS

AIM: To Study the Full – wave rectifier Circuit & to Find its, Ripple factor

EQUIPMENT:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer</td>
<td>9-0-9V/12-0-12V</td>
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<tr>
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<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Digital Multimeter</td>
<td>1kΩ,10kΩ</td>
<td>1</td>
</tr>
<tr>
<td>Resistor</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Connecting wires</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

THEORY:

The conversion of AC into DC is called Rectification. Electronic devices can convert AC power into DC power with high efficiency

FULL-WAVE RECTIFIER:

The full-wave rectifier consists of a center-tap transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D1 while a negative voltage appears at the anode of D2. Due to this diode D1 is forward biased it results in a current $I_{d1}$ through the load $R$.

During the negative half cycle, a positive voltage appears at the anode of D2 and hence it is forward biased. Resulting in a current $I_{d2}$ through the load at the same instant a negative voltage appears at the anode of D1 thus reverse biasing it and hence it doesn’t conduct.

MATHEMATICAL ANALYSIS (Neglecting $R_f$ and $R_s$)

The current through the load during both half cycles is in the same direction and hence it is the sum of the individual currents and is unidirectional

Therefore,

$$I = I_{d1} + I_{d2}$$

$$V_{ac} = V_m \sin \omega t$$
\[ I_{d1} = \frac{V_m}{R} \sin \omega t \quad 0 \leq \omega t \leq \pi \]
\[ = 0 \quad \pi \leq \omega t \leq 2\pi \]
\[ I_{d2} = 0 \quad 0 \leq \omega t \leq \pi \]
\[ = -\frac{V_m}{R} \sin \omega t \quad \pi \leq \omega t \leq 2\pi \]

The individual currents and voltages are combined in the load and therefore their average values are double that obtained in a half – wave rectifier circuit.

**AVERAGE OR DC VALUE OF CURRENT** $I_{dc}$

\[ I_{dc} = \frac{1}{2\pi} \left[ \int_{0}^{\pi} I_m \sin(\omega t) \, dt - \int_{\pi}^{2\pi} I_m \sin(\omega t) \, dt \right] = 2 \frac{I_m}{\pi} \]

Similarly,
\[ V_{dc} = 2V_m / \pi \]

**The RMS VALUE OF CURRENT**

\[ = \sqrt{\frac{1}{2\pi} \int_{0}^{\pi} I_m^2 \sin^2(\omega t) \, dt} \]
\[ = \frac{m}{\sqrt{2\pi}} \]

Similarly, \[ V_{rms} = \frac{V_m}{\sqrt{2\pi}} \]

**RIPPLE FACTOR**

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol $\gamma$
\[ \gamma = \frac{V_{ac}}{V_{dc}} \]
\[ (\gamma = 0.48) \]

**RECTIFICATION FACTOR**

The ratio of output DC power to the input AC power is defined as efficiency
Efficiency, $\eta$
\[ \eta = \frac{P_{dc}}{P_{ac}} = \frac{V_{dc} \cdot I_{dc}}{V_{ms} \sqrt{I_{ac}^2 + I_{dc}^2}} \times 100 \]

\[ \eta = 81\% \text{ (if } R >> R_f \text{, then } R_f \text{ can be neglected)} \]

Where \( R_f \) – forward resistance of two diode

**Peak – Inverse – Voltage (PIV)**

It is the maximum voltage that has to be withstood by a diode when it is reverse biased

\[ \text{PIV} = 2V_m \]

**Advantages of Full wave Rectifier**

1. \( \gamma \) is reduced
2. \( \eta \) is improved

**Disadvantages of Full wave Rectifier**

1. Output voltage is half the secondary voltage
2. Diodes with high PIV rating are used

Manufacturing of center-taped transformer is quite expensive and so Full wave rectifier with center-taped transformer is costly.

**CIRCUIT DIAGRAM (With out Filter):**

![Circuit Diagram](image)

**CIRCUIT DIAGRAM (With C -Filter):**

![Circuit Diagram](image)
PROCEDURE:
5. Make connections as per the Circuit Diagram.
6. Note down the AC and DC Voltages and Currents without Filter and with Load.
7. And again observe the AC and DC Voltages and Currents with Filter and with load.
8. Observe the Voltage across the secondary of the Transformer (i.e. \(V_{rms}\)).

Tabular Column:

<table>
<thead>
<tr>
<th>Condition</th>
<th>(V_{ac})</th>
<th>(V_{dc})</th>
<th>(V_m)</th>
<th>(R)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without Filter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>With C Filter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CALCULATIONS:
Ripple factor \(\gamma = \frac{V_{ac}}{V_{dc}}\)

Efficiency \(\eta = \frac{P_{dc}}{P_{ac}} = \frac{V_{dc} \times I_{dc}}{V_{rms} \sqrt{I_{ac}^2 + I_{dc}^2}} \times 100\)

Percentage of regulation = \(\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%\)

\(V_{NL}\) = Voltage across load resistance, When minimum current flows through it
\(V_{FL}\) = Voltage across load resistance, When maximum current flows through it.
EXPECTED WAVEFORMS:

Input Waveform

FULLWAVE RECTIFIER WITHOUT FILTER:

FULLWAVE RECTIFIER WITH FILTER:

\[ V_R = \text{Ripple Voltage} \]
RESULT:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without filter</th>
<th>With C Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple Factor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VIVA-VOCE Questions**

1. A diode should not be employed in the circuits where it is to carry more than its maximum forward current, why?

2. While selecting a diode, the most important consideration is its PIV, why?

3. The rectifier diodes are never operated in the breakdown region, why?

4. In filter circuits, a capacitor is always connected in parallel, why?
   In filter circuits, an inductor is always connected in series why?
Experiment No: 7

**FET CHARACTERISTICS**

**AIM:** To study Drain Characteristics and Transfer Characteristics of a FET.

**Components:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFET BFW 10</td>
<td>1</td>
</tr>
<tr>
<td>Resistors 470Ω</td>
<td>2</td>
</tr>
</tbody>
</table>

**Equipment:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>FET Trainer Kit</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td><strong>Digital Ammeter</strong></td>
<td>0-20mA</td>
<td>1</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>0-20 V</td>
<td>2</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Specifications:**

For **JFET BFW10:**
- Gate Source Voltage $V_{GS} = -30V$
- Forward Gain Current $I_{GF} = 10 mA$
- Maximum Power Dissipation $P_D = 300$ mW.

**Circuit Diagram:**

![Circuit Diagram](image-url)
Pin assignment of FET:

Source    Drain
          Gate
          Substrate

Theory:
The basic circuit diagram for studying drain and transfer characteristics is shown in figure.

Drain characteristics are obtained between the drain to source voltage ($V_{DS}$) and drain current ($I_D$) taking gate to source voltage ($V_{GS}$) as the parameter.

Transfer characteristics are obtained between the gate to source voltage ($V_{GS}$) and Drain current ($I_D$) taking drain to source voltage ($V_{DS}$) as parameter.

Procedure:

DRAIN CHARACTERISTICS

1. Make the connections as per circuit diagram.
2. Keep $V_{GS} = 0V$ by varying $V_{GG}$.
3. Varying $V_{DD}$ gradually, note down both drain current $I_D$ and drain to source voltage ($V_{DS}$).
4. Repeat above procedure (step 3) for $V_{GS} = -1V$.

TRANSFER CHARACTERISTICS:

1. Keep $V_{DS} = 2V$ by varying $V_{DD}$.
2. Varying $V_{GG}$ gradually from $0 - 5V$, note down both drain current ($I_D$) and gate to source voltage ($V_{GS}$).
3. Repeat above procedure (step 2) for $V_{DS} = 4V$.

Observations:

DRAIN CHARACTERISTICS:

<table>
<thead>
<tr>
<th></th>
<th>$V_{GS} = 0V$</th>
<th></th>
<th>$V_{GS} = -1V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$ (V)</td>
<td>$I_D$ (mA)</td>
<td>$V_{DS}$ (V)</td>
<td>$I_D$ (mA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Department of ECE, MIST
**TRANSFER CHARACTERISTICS:**

<table>
<thead>
<tr>
<th></th>
<th>$V_{DS} = 2V$</th>
<th></th>
<th>$V_{DS} = 4V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS}$ (V)</td>
<td>$I_D$ (mA)</td>
<td>$V_{GS}$ (V)</td>
<td>$I_D$ (mA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Graph (Instructions):**

1. Plot the drain characteristics by taking $V_{DS}$ on X-axis and $I_D$ on Y-axis at constant $V_{GS}$.
2. Plot the Transfer characteristics by taking $V_{GS}$ on X-axis and $I_D$ on Y-axis at constant $V_{DS}$.

**IN CHARACTERISTICS**

**Drain Resistance ($r_d$):** It is given by the ration of small change in drain to source voltage ($\Delta V_{DS}$) to the corresponding change in Drain current ($\Delta I_D$) for a constant gate to source voltage ($V_{GS}$), when the JFET is operating in pinch-off or saturation region.
Trans-Conductance ($g_m$): Ratio of small change in drain current ($\Delta I_D$) to the corresponding change in gate to source voltage ($\Delta V_{GS}$) for a constant $V_{DS}$.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}. \text{ (From transfer characteristics)}$$

The value of $g_m$ is expressed in mho’s (m) or siemens (s).

Amplification Factor ($\mu$): It is given by the ratio of small change in drain to source voltage ($\Delta V_{DS}$) to the corresponding change in gate to source voltage ($\Delta V_{GS}$) for a constant drain current.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}.$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_d \times g_m.$$

Inference:

1. As the gate to source voltage ($V_{GS}$) is increased above zero, pinch off voltage is increased at a smaller value of drain current as compared to that when $V_{GS} = 0 \, V$

2. The value of drain to source voltage ($V_{DS}$) is decreased as compared to that when $V_{GS} = 0 \, V$

Precautions:

1. While doing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
3. Do not switch ON the power supply unless you have checked the Circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals Of the FET.

Result:

1. Drain Resistance ($r_d$) = ...............
2. Transconductance ($g_m$) = ...............
3. Amplification factor ($\mu$) = ...............

Viva voce Questions

1. Why FET is called as a unipolar transistor?
2. What are the advantages of FET?
3. What is the difference between MOSFET and FET?
4. What is Trans conductance?
5. What is amplification factor?
6. Why thermal runaway does not occur in FET?
7. State weather FET is voltage controlled or current controlled and also state the reason?
8. State why BJT is current controlled device?
9. Why current gain is important parameter in BJT where as conductance is important Parameter in FET?
10. Why we plot input and output characteristics? What information we can obtain?
Experiment No:  8
DESIGN SELF BIAS CIRCUIT

AIM: Design a Self Bias Circuit For the following Specifications hfe = , Icq = 5mA, Vceq = 6.0 V, Vcc = 12.0 V, Rc = 1KΩ, S = 25.
Find the quiescent point (Operating Point) values of ICq and VCEq from the experiment and to find the maximum signal handling capability of the Amplifier

APPARATUS:

<table>
<thead>
<tr>
<th>S.No</th>
<th>Name</th>
<th>Range / Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Dual Regulated D.C Power supply</td>
<td>0–30 Volts</td>
</tr>
<tr>
<td>2</td>
<td>Transistor: BC107</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Capacitors: 50μf</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Capacitors: 10μf</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Multimeter</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Signal Generator: (0 – 1MHz)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Bread Board and connecting wires</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Dual Trace CRO</td>
<td>20MHz</td>
</tr>
</tbody>
</table>

CIRCUIT DIAGRAMS:

DESIGN PROCEDURE:

Icq = 5mA, Vceq = 6.0 V, Vcc = 12.0 V, Rc = 1KΩ, S = 25, Vbe=0.6 V.
Find hfe of the transistor
S = (1+β) / (1+βRe / (Re + Rb))
VB = VCCR2 / (R1 +R2)
RB = R1R2 / (R1+R2)
VB = IBRB + VBE + (1+β)IBRE
VCC = ICRc +VCE+(1+β)IBRE
Using the above formula find Re, R1, R2.
TABULAR FORM:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Theoretical Values</th>
<th>Practical Values</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_CE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_E</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PROCEDURE:
1. Connect the circuit as per the circuit diagram. Apply Vcc of 12 Volts DC.
2. Find the resulting DC Values of Icq and Vceq.
3. Apply a 1KHz signal from the Signal Generator and observe the O/P on CRO.
4. Increase the I/P voltage slowly until the output waveform starts distortion.
5. Note down the input voltage Vi at the point where the output starts distortion.
6. This input value is known as maximum signal handling capability.
7. Calculate the gain of the amplifier.

RESULT:
The maximum signal Handling capability of the amplifier = Volts
Gain of the amplifier =

PRECAUTIONS:
1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

VIVA QUESTIONS:
1. What is meant by Self Bias & fixed Bias circuits, Which one is preferred and why?
2. What is the significance of Emitter Resistance?
3. What is stability factor?
4. what is DC Load line and A.C. Load line?
5. what is quiescent point? What are the various parameters of the transistor that cause drift in q-point?
6. what are different techniques of stabilization?
7. Relate stability factor with the circuit parameters.
8. What is the relation between α and β.
9. If bypass capacitor is removed ,what happens to the gain?

***
Experiment No:  9
COMMON COLLECTOR AMPLIFIER

AIM: - To Study the common collector amplifier and to find
1. Cut off frequencies.
2. Bandwidth.

Components:

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor BC 107</td>
<td>1</td>
</tr>
<tr>
<td>Resistors 10KΩ,33KΩ,8.2KΩ,2.2KΩ</td>
<td>1</td>
</tr>
<tr>
<td>Capacitors 10μf</td>
<td>2</td>
</tr>
</tbody>
</table>

EQUIPMENT REQUIRED:

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>1</td>
</tr>
<tr>
<td>CRO</td>
<td>1</td>
</tr>
<tr>
<td>Function generator</td>
<td>1</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
</tr>
</tbody>
</table>

THEORY:

In common collector amplifier as the collector resistance is made to zero, the Collector is at ac ground that is why the circuit is also called as grounded Collector amplifier or this configuration is having voltage gain close to unity And hence a change in base voltage appears as an equal change across the Load at the emitter, hence the name emitter follower. In other words the Emitter follows the input signal.

This circuit performs the function of impedance transformation over a wide range of frequencies with voltage gain close to unity. In addition to that, the emitter follower increases the output level of the signal. Since the output voltage across the emitter load can never exceed the input voltage to base, as the emitter-base junction would become back biased. Common collector state has a low output resistance, the circuit suitable to serve as buffer or isolating amplifier or couple to a load with large current demands.

Characteristics of CC amplifier:

1. Higher current gain
2. Voltage gain of approximately unity
3. Power gain approximately equal to current gain
4. No current or voltage phase shift
5. Large input resistance
6. Small output resistance
CIRCUIT DIAGRAM:

PROCEDURE:
1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage $V_s = 50$ mV (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant vary the frequency from 50Hz to 1MHz in regular steps.
   And note down the corresponding output voltage.
4. Plot the Graph: Gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.

Graph (Frequency Response):

TABULAR COLUMN: $V_s = 50$ mV
In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as \( f_L \) and \( f_H \), and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth (\( f_H - f_L \)).

**RESULT:**

Maximum Gain=
3db Gain= Maximum Gain -3db

Band Width =

**Viva Voce Questions**

1. Why CC amplifier is known as emitter follower?
2. Mention the applications of CC amplifier. Justify?
3. What is the phase difference between input and output signals in the case of CC amplifier?
4. Mention the characteristics of CC amplifier?
5. What is gain bandwidth product?

<table>
<thead>
<tr>
<th>Frequency</th>
<th>( V_o ) (volts)</th>
<th>Gain = ( V_o/V_s )</th>
<th>Gain (dB) = (20 \log_{10} V_o/V_s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Experiment No: 10
COMMON EMITTER AMPLIFIER

AIM: - To Study the common emitter amplifier and to find
1. Cut off frequencies.
2. Bandwidth.

Components:

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor BC 107</td>
<td>1</td>
</tr>
<tr>
<td>Resistors 10KΩ(2),33KΩ,1KΩ</td>
<td>1</td>
</tr>
<tr>
<td>Capacitors 10µf</td>
<td>2</td>
</tr>
<tr>
<td>4.7 µf (1)</td>
<td></td>
</tr>
</tbody>
</table>

EQUIPMENT REQUIRED:

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>1</td>
</tr>
<tr>
<td>CRO</td>
<td>1</td>
</tr>
<tr>
<td>Function generator</td>
<td>1</td>
</tr>
<tr>
<td>Connecting wires</td>
<td></td>
</tr>
</tbody>
</table>

THEORY:
The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.

Resistors $R_1$ & $R_2$ form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter - base junction is operating in the proper region.

In order to operate transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design the $V_{CE}$ is always set to $V_{CC}/2$. This will conform that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. Output is produced without any clipping or distortion for the maximum input signal. If not so, reduce the input signal magnitude.

The Bypass Capacitor The emitter resistor $R_E$ is required to obtain the DC quiescent stability. However the inclusion of $R_E$ in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} \ll R_E$$

$$\frac{1}{2\pi f C_E} \ll R_E$$
$$C_E \gg \frac{1}{2\pi f R_E}$$

**The Coupling Capacitor** An amplifier amplifies the given AC signal. In order to have noiseless transmission of signal (without DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between any two stages.

$$X_{CC} \ll (R_i \text{ hie})$$

$$\frac{1}{2\pi f C_C} \ll (R_i \text{ hie})$$

$$C_C \gg \frac{1}{2\pi f C_C (R_i \text{ hie})}$$

**Frequency Response** Emitter bypass capacitors are used to short circuit the emitter resistor and thus increase the gain at high frequency. The coupling and bypass capacitors cause the fall of in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitors are effectively open circuits.

In the mid frequency range the large capacitors are effective short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence, the mid band gain is maximum.

At the high frequencies, the bypass and coupling capacitors are replaced by short circuits and stray capacitors and the transistor determine the response.

**Circuit Diagram:**

![Circuit Diagram](image)

**Procedure:**

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage $V_s = 50$ mV (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.
4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.
6. Calculate all the parameters at mid band frequencies (i.e. at 1 KHz).

**Graph (Frequency Response):**

**TABULAR COLUMN:**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>V_o (volts)</th>
<th>Gain = V_o/V_s</th>
<th>Gain (dB) = 20 log (V_o/V_s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

V_s = 50mV

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L and f_H, and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth (f_H – f_L).

**RESULT**

Maximum Gain=
3db Gain = Maximum Gain -3db
Band Width =

**Reasoning Questions**

1. How do we test the transistor for active region condition?
2. What are the factors, which influence the higher cut-off frequency?
3. What are the components, which influence the lower cut-off frequency?
4. Mention the applications of CE amplifier. Justify?
5. Compare the characteristics of CE amplifier, CB amplifier & CC amplifier.
6. What must be the voltage across the transistor, when it is operated as a switch?
7. How do we test the transistor for switching condition?
Experiment No: 11
COMMON SOURCE FET AMPLIFIER

AIM: - To Study the JFET Common Source amplifier and to find
1. Bandwidth
2. Cut off frequencies.

EQUIPMENT REQUIRED:

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Source JFET amplifier Kit</td>
<td>(0-20) MHz</td>
<td>1</td>
</tr>
<tr>
<td>CRO</td>
<td>(0-1) MHz</td>
<td>1</td>
</tr>
<tr>
<td>Function generator</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Connecting wires</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

THEORY:
The possible three configurations of JFET amplifiers, common source (CS) Configuration is mostly used. The advantage of using CS configuration is that it has very high input impedance. Figure (1) shows the FET amplifier of common source configuration. The biasing input and couplings are shown in the figure. The midrange voltage gain of the amplifier is given by

\[ A = g_m \left( r_d \parallel R_L \right) \]

At the mid-frequency range, there is no effect of input and output coupling capacitors. Therefore, the voltage gain and phase angle are constant in this frequency range. The amplifier shown in figure (1) has only two RC networks that influence its low-frequency response. One network is formed by the output coupling capacitors and the output impedance looking in at the drain. Just as in the case of BJT amplifier, the reactance of the input coupling capacitor, reactance increases as the frequency decreases. The phase angle also changes with change in frequency.

As the frequency is increased beyond mid-frequency range the internal transistor capacitance effect is predominant. For JFETs, \( C_{gs} \) is the internal capacitance between gate and source. This is also called input capacitance, \( C_{iss} \). The other internal capacitance, which effects the performance is \( C_{gd} \) acts as a feedback circuit, which couples both, input and output. The effect of both these capacitances is that it reduced the gain appreciably as in the case of BJT.
CIRCUIT DIAGRAM:

![Circuit Diagram]

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage $V_s = 50$ mV (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.
4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.
6. Calculate all the parameters at mid band frequencies (i.e. at 1 KHz).
7. To calculate Voltage Gain:

   \[ \text{Voltage Gain} (A_{VS}) = \frac{\text{Output Voltage} (V_o)}{\text{Source Voltage} (V_s)} \]
Graph (Frequency Response)

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$V_o$ (volts)</th>
<th>Gain = $V_o/V_s$</th>
<th>Gain (dB) = $20 \log (V_o/V_s)$</th>
</tr>
</thead>
</table>

**TABULAR COLUMN:** $V_S = 50mV$

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain ($|A|$ max). These are shown as $f_L$ and $f_H$, and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth ($f_H - f_L$).

**RESULT:**

Maximum Gain=
3db Gain= Maximum Gain -3db
Band Width =
**Reasoning Questions**

1. What are the advantages of FET amplifier over conventional transistor amplifiers?

2. Voltage gain of a FET is less than a BJT, Why?

3. FET is used as a buffer amplifier, why?

4. Input impedance of MOSFET is much higher than a FET, Why?

5. A MOSFET can be operated with positive or negative gate voltage, why?
Experiment No: 12

SCR CHARACTERISTICS

OBJECTIVE: To plot Volt-Ampere Characteristics of SCR.

EQUIPMENT:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>SCR</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Regulated Power Supply</td>
<td>0-30V DC</td>
<td>2</td>
</tr>
<tr>
<td>Digital Ammeter</td>
<td>0-200μA/200mA</td>
<td>1</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>0-20V DC</td>
<td>1</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

THEORY:

SCR is a four layer three junction PNPN silicon semiconductor switching device. It has a 3 terminals anode, cathode and gate. SCR stands for Silicon Controlled Rectifier. It acts as a switch when forward biased. When the gate is kept open i.e., gate current \( I_G = \text{0} \), operation of SCR is similar to PNPN diode. When \( I_G \) is less than zero, the amount of reverse bias applied to \( J_2 \) is increased. So the break over voltage \( V_{BO} \) is increased. When \( I_G \) is greater than zero, the amount of reverse bias applied to \( J_2 \) is decreased thereby decreasing the break over voltage with very large positive gate current break over may occur at a very low voltage such that the characteristics if SCR is similar to that of a PN diode. As the voltage at which the SCR is switched ‘ON’ can be controlled by varying the gate current \( I_G \), it is commonly called as controlled switch. Once SCR is ON, the gate loses control, i.e. the gate cannot be used to switch the device OFF. One way to turn the device OFF is by lowering the anode current below the holding current \( V_{H} \), keeping the gate open.

SCR is used in relay control, motor control, phase control, heater control, battery chargers, inverters, regulated power supplies and as static switches.
PROCEDURE:
1. Make connections as shown in circuit diagram.
2. By increasing $V_{GG}$ set the gate current to $I_G$ say (40 $\mu$A), go on increasing the plate
   Supply voltage $V_{BB}$ and read this voltage $V_{AK}$ across anode and cathode. When this
   Voltage is equal to the firing voltage ($I_f$) of SCR, the voltmeter suddenly deflects back
   To low value (say<1) and the SCR fires and anode current suddenly jumps and is read
   By multimeter $I_A$. Note down the reading of the volt-meter when it deflects back and at
   This point the anode current is approximately equal to zero.
3. After deflection of voltmeter to approximately 1V note down this voltage and
   Corresponding anode current. Now further increase the anode supply voltage $V_{BB}$ and
   Note down the corresponding anode current $I_A$ and anode to cathode voltage $V_{AK}$.
   Repeat this process until $V_{BB} = 30V$ and tabulate the result.
4. Repeat the above procedure for different gate currents $I_G$ and tabulate the readings.
5. Now plot the V-I characteristics in a graph by taking $V_{AK}$ along x-axis and $I_A$ along y-
   Axis.
OBSERVATIONS:

<table>
<thead>
<tr>
<th>$I_G = 40\mu A$</th>
<th>$I_G = 50\mu A$</th>
<th>$I_G = 60\mu A$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{AK}$ (Volts)</td>
<td>$I_A$ (mA)</td>
<td>$V_{AK}$ (Volts)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

EXPECTED GRAPH:

![Graph showing $I_A$ (mA) vs $V_{BO}$ to $V_{AK}$ (Volts)]

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the SCR. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULT: The V-I characteristics of the SCR was plotted.
VIVA-VOCE QUESTIONS

1. What are the applications of SCR?
2. How can a SCR be turned OFF?
3. Explain the negative resistance characteristic of SCR?
Experiment No: 13

**UJT CHARACTERISTICS**

**Objective:** To study and plot the emitter characteristics ($V_E$ vs $I_E$) of a UJT.

**Components:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>UJT</td>
<td>1No</td>
</tr>
<tr>
<td>Resistors 1KΩ</td>
<td>2No</td>
</tr>
</tbody>
</table>

**Equipment:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bread Board</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>UJT</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Regulated Power Supply</td>
<td>0-30V DC</td>
<td>2</td>
</tr>
<tr>
<td>Digital Ammeter</td>
<td>0-20mA</td>
<td>1</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>0-20V/30V DC</td>
<td>1</td>
</tr>
<tr>
<td>Connecting Wires</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Specifications:**

For UJT 2N – 2646:

- Peak Emitter Current ($I_P$) = 2A
- Continuous Emitter Current ($I_E$) = 50mA
- Inter Base Voltage ($V_{BB}$) = 35V
- Emitter Base Reverse Voltage ($V_{EB2}$) = −30V
- Power Dissipation at 25°C = 300mW

**Circuit Diagram:**

![Circuit Diagram](image-url)
Pin assignment of UJT:

The Uni-junction transistor is a 3-terminal solid-state device (emitter and the Two bases). Fig (a) shows the symbol of UJT. A simplified equivalent circuit Is shown in fig (b).

Fig (a): Symbol of UJT  Fig (b): Equivalent Circuit

This device has only one pn junction and hence it is known as Uni-junction transistor. The PN emitter to base junction is shown as diode D1. The inter base resistance R_{BB} of the N-type Si bar appears as two resistors R_{B1} & R_{B2} where R_{BB} equals the sum of R_{B1} & R_{B2}.

Referring to the equivalent circuit

I. When no voltage is applied between B1 and B2 with emitter open, the inter base resistance is given by R_{BB} = R_{B1} + R_{B2}.

II. When a voltage V_{BB} is applied between B1 and B2 with emitter open, voltage will divide up across R_{B1} & R_{B2}.

\[ V_{RB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \times V_{BB}, \quad \frac{V_{RB1}}{V_{BB}} = \frac{R_{B1}}{R_{B1} + R_{B2}} \]

\[ V_{RB1} = \eta V_{BB} \quad \text{where} \quad \eta = \text{the intrinsic stand-off ratio} = \frac{R_{B1}}{R_{B1} + R_{B2}} \]

The \eta V_{BB} across R_{B1} reverse biased diode thereby dropping the emitter current to zero.

III. When supply is connected at the emitter, the diode is forward biased making the input voltage to exceed by V_{D}

\[ V_{P} = \eta V_{BB} + V_{D} \]
The emitter conductivity characteristics are such that as $I_E$ increases the emitter to base (B1) voltage decreases. At a peak point $V_p$ and the valley point $V_v$, the slope of the emitter characteristics is 0. At points to the left of $V_B$ the E-B1 is forward biased and $I_E$ exists. Between $V_p$ & $V_v$, increase in $I_E$ is accompanied by a reduction in emitter voltage $V_E$. This is the negative resistance region of UJT. Beyond the valley point $V_v$, an increase in $I_E$ is accompanied by an increase in $V_E$. This region is known as the saturation region.

**Procedure:**

1. Make the connections as per circuit diagram.
2. Keep output voltage $V_{BB} = 5V$ by varying $V_{BB}$.
3. Varying $V_{EE}$ gradually, note down both emitter current $I_E$ and emitter voltage ($V_E$).
4. Step Size is not fixed because of non-linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
5. Repeat above procedure (step 3) for $V_{BB} = 10V$.

**Observations:**

<table>
<thead>
<tr>
<th>$V_{BB}$ = 5V</th>
<th>$V_{BB}$ = 10V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_E$ (mA)</td>
<td>$V_E$ (V)</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Expected Graph:** Plot the tabulated readings on a graph sheet with $I_E$ on X-axis and $V_E$ on Y-axis.
**Inference:**

1. There is a negative resistant region from peak point to valley point.
2. Increase in $V_{BB}$ increases the value of peak and valley voltages.

**Precautions:**

1. While doing the experiment do not exceed the ratings of the UJT. This may lead to damage the UJT.
2. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
3. Do not switch ON the power supply unless you have checked the Circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base -1 and base – 2 terminals Of the UJT.

**Result:** The emitter characteristics of UJT have been determined.

**Viva-voce Questions**

1. Specifications of UJT?
2. What is the importance of UJT?
3. When will be UJT is switched?
4. Why UJT is called as a relaxation oscillator?
5. What is a Relaxation Oscillator?
ADDITIONAL EXPERIMENTS

Experiment No: 1

MEASUREMENT OF h-PARAMETERS OF A TRANSISTOR

AIM: To calculate the hybrid parameters of transistor in CE, CC, CB configurations.

Equipment Required:

Semiconductor trainer module containing:-
- Bread board
- 0-15V power supplies – 2 No’s.
- AC power 12-0-12V
- Digital voltmeter 0-20V DC
- Digital ammeter 0-20µA/mA DC

Components Required:
- Transistor BC 107
- Resistors 1KΩ – 2 No’s.

Rating of the BC 107 transistor
- $I_C$ (max) = 200mA
- $V_{CEO}$ = 45 V
- $P_{TOT}$ = 300mW
- $T_J$ = 175d.c.
- NPN transistor

Theory:

The terminals behavior of a two port large scale network is specified by two voltages and two currents. We may select two of the four quantities as independent variables and express the remaining two in terms of the chosen independent variables. The typical representation of a two port network is shown in Fig. 801.

If the current $i_1$ and voltage $v_2$ are the independent parameters and if the two ports are linear, we may write:

$$V_1 = h_{11}i_1 + h_{12}v_2$$

$$I_2 = h_{21}i_1 + h_{22}v_2$$
The quantities $h_{11}$, $h_{12}$, $h_{21}$, and $h_{22}$ are called h-or hybrid parameters because all are not alike dimensionally but are hybrid in nature i.e., combinations of admittance, impedance and dimensionless quantities.

The basic assumption in deriving h-mode for a transistor is that the variations about the quiescent point are small so that the transistor parameters can be considered constant over the signal excursion. In order to derive transistor hybrid model, we consider the CE circuit. The voltages and currents related to input and output ports of a transistor respectively in CE configuration are $v_b$, $i_b$ and $v_c$, $i_c$. Hence the h-parameter equations related to transistor can be written as:

$$V_b = h_{ie}i_b + h_{re}v_c$$
$$I_C = h_{fe}i_b + h_{oe}v_c$$

Where

$$h_{ie} = \frac{\partial v_b}{\partial i_b} \bigg|_{v_c} , \quad h_{re} = \frac{\partial v_b}{\partial v_c} \bigg|_{i_b} ,$$
$$h_{fe} = \frac{\partial i_c}{\partial i_b} \bigg|_{v_c} , \quad \text{and} \quad h_{oe} = \frac{\partial i_c}{\partial v_c} \bigg|_{i_b} ,$$

Calculation of h-parameters from the family of input and output parameters for CE configuration is explained below.

$h_{fe}$: From the definition $h_{fe}$ is the short circuited forward current grain and is a dimensionless parameter. This parameter can be calculated from the graph as follows.

$$h_{fe} = \frac{\Delta i_c}{\Delta i_B} \bigg|_{v_c} = \frac{i_{c2} - i_{c1}}{i_{B2} - i_{B1}}$$

The current increments are taken around Q point, which corresponds to base current $I_B=i_B$ and $V_{CE}=V_c$.

$H_{fe} = \beta' = \text{small signal current gain and}$

$B = h_{fe} = \text{large signal current gain.}$

$h_{oe}$: It gives the output admittance with input open circuited and the units are ohms. This parameter can be calculated from the graph using the formula given below.

$$h_{oe} = \frac{\Delta i_c}{\Delta v_c} \bigg|_{i_b} = \frac{i_{c2} - i_{c1}}{v_{c2} - v_{c1}}$$

The above two h-parameters can be calculated from the family of output characteristics of the given configuration. We can calculate other two h-parameters from the family of input characteristics as explained below.
\textbf{h}_{e}: \text{ It is defined as open circuited reverse voltage gain and is a dimensionless quantity. This parameter can be calculated from the graph using the formula given below.}

\[ h_e = \frac{\partial v_B}{\partial v_c} \approx \frac{\Delta v_B}{\Delta v_c} \bigg|_{i_B} = \frac{v_{B_2} - v_{B_1}}{v_{c_2} - v_{c_1}} \]

\textbf{\( h_{oe} \): By definition \( h_{oe} \) represents input impedance when output terminals are short circuited and its units are ohms. It can be calculated using formula given below.}

\[ h_{oe} = \frac{\partial v_B}{\partial i_B} \approx \frac{\Delta v_B}{\Delta i_B} \bigg|_{v_e} = \frac{v_{B_2} - v_{B_1}}{i_{B_2} - i_{B_1}} \]

**Circuit Diagram:**

![Circuit Diagram](image)

**Procedure:**

1. Connect a common emitter transistor configuration circuit for plotting its input characteristics as shown in fig.8.3.
2. Take a family of readings for variation in \( I_B \) with \( V_{EB} \) at different fixed values of output voltage \( V_{CE} \).
3. Tabulate the readings and plot the input characteristic curves of CE configuration.
4. From the graphs, calculate the input resistance \( h_{ie} \) and reverse voltage transfer ratio \( h_{re} \) by taking the slopes of the curves and using the formulate given in the theory above.
5. Tabulate the reading in Table 1.
6. Take the family of readings for variation of \( I_c \) with \( V_{CE} \) at different values of \( I_B \).
7. Tabulate readings and plot the output characteristic curves.
8. From the graphs, calculate \( h_{ie} \) and \( h_{re} \) by taking the slopes of the curves.
9. Tabulate the readings in Table 1.

Graph:
I. From input characteristics:

\[
\begin{align*}
\text{a) Input impedance } h_{ie} &= \frac{\Delta V_{BE}}{\Delta I_B} \bigg|_{V_{CE}=V} \\
&= \frac{X_2 - X_1}{Y_2 - Y_1} \Omega
\end{align*}
\]

\[
\begin{align*}
\text{b) Reverse transfer voltage gain } h_{re} &= \frac{\Delta V_{BE}}{\Delta V_{CE}} \bigg|_{I_B \text{ const}}; \\
&= \frac{X_2 - X_1}{Y_2 - Y_1} = h_{re} \Omega
\end{align*}
\]
II. From output characteristics:

(a) Forward transfer current ratio:

\[ h_{fe} = \frac{\Delta I_C}{\Delta I_B} |V_{ce}|_{const}; \]

i.e. \[ h_{fe} = \frac{Y_2 - Y_1}{X_2 - X_1} \]

Output conductance

\[ h_{oc} = \frac{\Delta I_C}{\Delta I_{CE}} |I_B|_{const}; \]

\[ h_{oc} = \frac{Y_2 - Y_1}{X_2 - X_1} V. \]
<table>
<thead>
<tr>
<th>Sino.</th>
<th>h parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Current gain, $h_{fe}$</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Output Admittance, $h_{oe}$</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reverse voltage gain, $h_{re}$</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Input impedance, $h_{ie}$</td>
<td></td>
</tr>
</tbody>
</table>

Table – 1.

**Result:**

The h parameters for a transistor in CE configuration are calculated.

1. Input Impedance $h_{ie} =$ ohms
2. Reverse transfer voltage gain $h_{re} =$
3. Forward transfer current ratio $h_{fe} =$
4. Output conductance $h_{oe} =$ mhos.

**Viva-Voce Questions**

1. What is the range of values of Input Impedance $h_{ie}$ in CB CE, CC and why?
2. What is the range of values of Reverse transfer voltage gain $h_{re}$ in CB, CE, CC and why?
3. What is the range of values of Forward transfer current ratio $h_{fe}$ in CB, CE, CC and why?
4. What is the range of values of Output conductance $h_{oe}$ in CB CE, CC and why?
BRIDGE RECTIFIERS

AIM: To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full-wave Bridge rectifier circuit with and without Capacitor filter.

APPARATUS:

<table>
<thead>
<tr>
<th>S.No</th>
<th>Name</th>
<th>Range / Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Transformer</td>
<td>230V / 0-9V</td>
</tr>
<tr>
<td>2</td>
<td>Diode</td>
<td>1N4001</td>
</tr>
<tr>
<td>3</td>
<td>Capacitors</td>
<td>1000μF/16V, 470μF/25V</td>
</tr>
<tr>
<td>4</td>
<td>Decade Resistance Box</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>Multimeter</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>Bread Board and connecting wires</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>Dual Trace CRO</td>
<td>20MHz</td>
</tr>
</tbody>
</table>

PROCEDURE:

WITHOUT FILTER:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the $R_L$ value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 1KΩ and note down the $V_{ac}$ and $V_{dc}$ as per given tabular form
5. Disconnect load resistance (DRB) and note down no load voltage $V_{dc}$ ($V_{no load}$)
6. Connect load resistance at 1KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
7. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of Regulation, $\% \eta = \frac{V_{no load} - V_{full load}}{V_{no load}} \times 100\%$

WITH CAPACITOR FILTER:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.
**Tabular Column:**

\[ V_{ac} = \_\_\_\_ \text{ (Voltage across the secondary of the transformer)} \]

<table>
<thead>
<tr>
<th>Condition</th>
<th>( V_{ac} )</th>
<th>( V_{dc} )</th>
<th>( V_{m} )</th>
<th>( R )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without Filter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>With C Filter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**RESULT:** Observe Input and Output Waveforms and Calculate ripple factor and percentage of regulation in Full-wave Bridge rectifier with and without filter.

**Without Filter:**
- Ripple Factor :
- Regulation :

**With Capacitor Filter:**
- Ripple Factor :
- Regulation :

**PRECAUTIONS:**
1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

**VIVA QUESTIONS:**
1. What are the advantages of Bridge Rectifier over the center tapped Rectifier?
2. What does Regulation indicate?